HW#5

CSc 137

Problem I: Consider the sequential circuit in Figure 5.31 where the adder is a CLA. Its simplified circuit is shown in Figure 5.32. Assuming that the Flip-Flips register set-up time, clock-to-q, and clock-skew are each 0.1 ns, determine the upper bound for its clock frequency. (4 pts)

Problem II: Textbook problem 5.9 assuming the unknown state are ignored (don’t care) in the design. (5 pts)

Problem III: Textbook problem 5.11 (only FSD) (3 pts)